Amendments to the Claims:

1. (currently amended) A high electron mobility transistor (HEMT) comprising:

a channel layer being composed of a II-VI compound semiconductor zinc oxide;

a gate [[electrode]] contact disposed on said channel layer; and

a gate insulating [[film]] layer disposed between said gate [[electrode]] contact and said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure.

2. (currently amended) A HEMT according to claim 1 wherein said gate insulating [[film]] layer is composed of at least one of an epitaxially grown Group-III nitride compound semiconductor and a MgZnO quantum well structure.

3. (original) A HEMT according to claim 2 wherein said channel layer is composed of an epitaxially grown Group-II-VI zinc oxide compound semiconductor.

4. (currently amended) A HEMT according to claim 1 wherein said gate insulating [[film]] layer is composed of a Group-III compound semiconductor expressed by a chemical formula $Al_x Ga_{1-x} N$ ($0.3<x.\leq 1$) or $Mg_xZn_{1-x} O$ ($0.1<[[x.]]x<.4$).

5. (currently amended) A HEMT according to claim 1 wherein said channel layer is formed on a substrate [[comprises]] comprising at least one of zinc oxide (ZnO), silicon carbide (SiC), sapphire (Al_2O_3), and silicon (Si) and has a bulk resistivity higher than 10^5 ohm-centimeter (Ω-cm).

6. (currently amended) A HEMT according to claim 1 wherein the thickness of said gate insulating [[film]] layer ranges from 0.30 nanometer (nm) to 50 nm.

7. (currently amended) A HEMT according to claim 1 wherein said HEMT employs piezoelectric doping created by strain due to lattice mismatch between the channel layer and the gate insulating layer that produces a two-dimensional electron gas (2DEG) near [[the]] an interface between the channel layer and the gate insulating layer to avoid [[avoiding the]] usage of a conventional doping method.

8. (original) A HEMT according to claim 1 wherein said gate contact is [[a rectifying contact]] selected from the group consisting of titanium (Ti), platinum (Pt), silver (Ag), gold (Au), chromium (Cr), alloys of titanium(Ti) and tungsten (W), and platinum silicide (PtSi).

9. (currently amended) A HEMT according to claim 1 wherein [[said]] source and drain contacts to said channel layer comprise an alloy of titanium (Ti), silicon (Si), aluminum (Al) and nickel (Ni).

10. (currently amended) A HEMT according to claim 1 and further comprising a passivation layer on said gate contact and [[said rectifying contacts and on said heterojunction]] said source and drain contacts to said channel layer.

11. (currently amended) A HEMT according to claim 1 wherein said gate [[electrode]] contact [[has side walls on the lateral surfaces thereof]] is bounded by side walls of said gate insulating layer.

12. (currently amended) A HEMT according to claim [[1]] 11 wherein [[the contact]] an area of said gate [[electrode]] contact with said [[gate-insulating film]] gate insulating layer is decreased due to the presence of said sidewalls.

13. (currently amended) A HEMT according to claim 1 wherein the [[a]] channel layer is composed of ZnO and is grown by metal organic chemical vapor deposition (MOCVD).

14. (currently amended) A HEMT according to claim 1 wherein gate insulating [[film]] layer is grown by metal organic chemical vapor deposition (MOCVD) and sequentially laminated on [[a ZnO]] said channel layer, and the [[ZnO]] channel layer in turn is laminated onto a [[ZnO]] substrate, said channel layer and said substrate composed of ZnO.

15. (currently amended) A HEMT according to claim 14 wherein the [[ZnO]] substrate is a c-surface substrate.

16. (canceled)

17. (currently amended) A method comprising:

defining a channel layer composed of a II-VI compound semiconductor zinc oxide;

forming a gate [[electrode]] contact disposed on said channel layer; and

forming a gate insulating [[film]] layer disposed between said gate [[electrode]] contact and said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure.

18. (currently amended) A method according to claim 17 wherein the gate insulating [[film]] layer is formed by metal organic chemical vapor deposition (MOCVD).

19. (currently amended) A method according to claim 17 wherein the channel layer is formed on a [[ZnO]] substrate [[is]] comprising a c-surface ZnO substrate.

20. (canceled)